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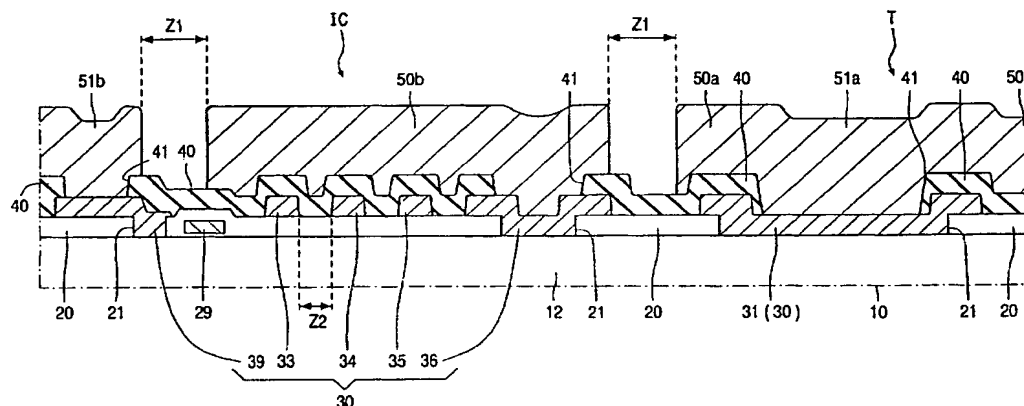
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(54) Title: RESIN SEALED SEMICONDUCTOR DEVICE WITH STRESS-REDUCING LAYER



(57) Abstract: Thermal cycling can lead to damaging stress at the upper surface of a semiconductor device chip (10) encapsulated in synthetic resin material (100), particularly in the case of power devices that include an IC. The invention provides a thick ductile layer pattern (50) of, for example, aluminium over most of the top surface of the insulating over-layer (40) of the chip (10). Electrically-isolated parts (50a, 50b, 50c, 50d etc.) of this ductile covering are individually connected to respective underlying conductive areas so as to reduce charging effects across the insulating over-layer (40). A sufficient spacing Z1 is present between these isolated parts (50a, 50b, 50c, 50d etc.) to avoid short circuits as a result of deformation by shearing and smearing during thermal cycling of the device. The ductile metal layer pattern (50) reduces stress between the insulating material (40) and the plastic material (100), but it can be both easily and cheaply applied in device manufacture before dividing the wafer into individual chips.